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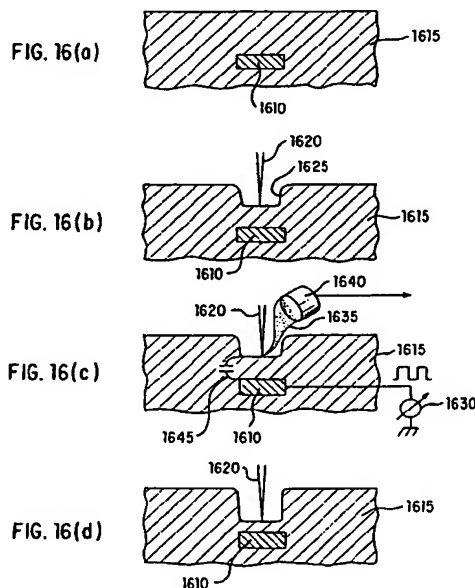
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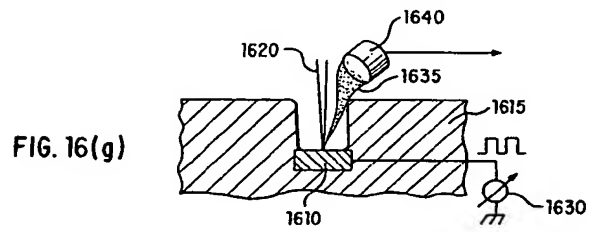
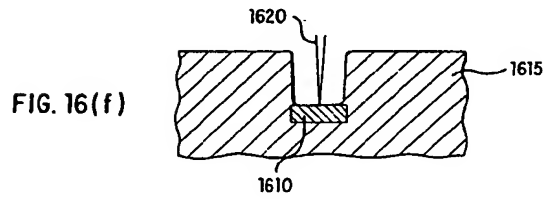
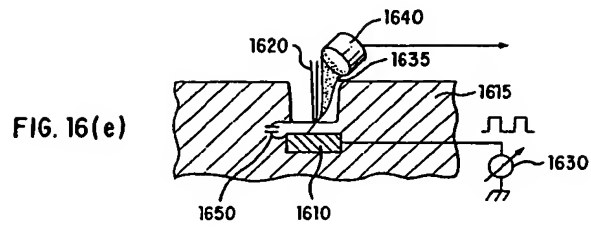
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Integrated circuits modification with focused ion beam system.

Apparatus is provided which includes a FIB column having a vacuum chamber for receiving an IC, means for applying a FIB to the IC, means for detecting secondary charged particles emitted as the FIB is applied to the IC, and means for electrically stimulating the IC as the FIB is applied to the IC. The apparatus may be used, for example, (1) to locate a conductor buried under dielectric material within the IC, (2) for determining milling end-point when using the FIB to expose a buried conductor of the IC, and (3) to verify the repair of an IC step-by-step as the repair is made.



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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to focused ion beam (FIB) methods and systems useful, for example, in failure analysis of Very Large Scale Integrated (VLSI) circuit devices. In particular, the present invention relates to methods and systems in which a FIB is employed in locating, milling, and/or depositing conductors within an integrated circuit.

2. The Prior Art

Time-to-market often determines the economic success or failure of new IC devices in the semiconductor industry. Reducing the debug and verification time for new IC designs provides an important competitive advantage. Systems based on Focused Ion Beam (FIB) technology and electron-beam (e-beam) technology are increasingly important in debug and verification as IC design rules shrink below 1 μm .

Systems based on FIB technology are gaining widespread acceptance in the semiconductor industry in a broad range of applications including IC repair, failure analysis and process monitoring. See, for example, K. NIKAWA, *Applications of Focused Ion Beam Technique to Failure Analysis of VLSIs: a Review*, Paper presented at the SECOND JAPAN-US SEMINAR ON FOCUSED ION BEAM APPLICATIONS, December 1990. A number of general purpose commercial FIB systems are available, but none so far is believed to have an architecture tailored specifically to the needs of the semiconductor industry.

FIB systems are conventionally used to perform three major functions: (1) etching/milling of structure, such as for cutting metal lines and drilling holes, (2) depositing material, such as for forming metal connectors and pads, and (3) scanning ion microscope (SIM) observation. These functions may be employed to modify the IC for failure analysis. For example, cutting and connecting metal lines aids in confirmation of an suspected failure mechanism or failure location, and milling holes in an insulation layer allows a "buried" conductor to be exposed or connected to a pad for improved e-beam or mechanical probing.

However, FIB systems currently in use have significant limitations. In semiconductor fabrication processes where inter-layer dielectric material is used to planarize the IC's surface, conductors buried underneath the surface are often not visible in a conventional SIM image. Milling through the dielectric material to expose a buried conductor poses the difficulty of precisely positioning the FIB

over the conductor without being able to observe the conductor.

The FIB IC repair success rate is well known to be poor (typically <50%) particularly when IC modifications are complex or extensive. It is often necessary to modify three devices to obtain one device which works; a small increase in the success rate of modification can thus dramatically increase the time required to obtain a single functioning device. The milling process is sufficiently imprecise that it is possible to mill too deeply and cut through the conductor or mill too little and fail to expose the conductor. The result can be unintended open circuit within the modified IC. Unreliable end-point detection, i.e., unreliable determination of when to terminate the milling process, particularly on lower level conductors, is frequently cited as the key issue in failed repairs.

Repair of an IC may involve making multiple modifications, reducing the odds of success. Verifying that a repair has been correctly made involves removing the IC from the FIB system and, typically, placing it in an e-beam system where it may be stimulated and probed. Overall, the repair and verification process can be time-consuming and yield uncertain results.

In recent years, voltage-contrast electron-beam (e-beam) probing has gained broad acceptance in the semiconductor industry for applications including IC design debug and verification, failure analysis and characterization. See, for example, N. RICHARDSON, *E-Beam Probing for VLSI Circuit Debug*, VLSI SYSTEMS DESIGN, August 1987. E-beam probing systems and techniques allow signals on internal nodes of an operating IC to be probed, using the principle of voltage contrast in a scanning electron microscope (SEM). A focused beam of primary electrons is directed toward a conductor within a circuit specimen as signals are applied to the specimen. Detected secondary electrons are indicative of the surface electrical potential on conductors within the specimen. See, for example, E. Menzel & E. Kubalek, *Fundamentals of Electron Beam Testing of Integrated Circuits*, 5 SCANNING 103-122(1983), and E. Plies & J. Otto, *Voltage Measurement Inside Integrated Circuit Using Mechanical and Electron Probes*, IV SCANNING ELECTRON MICROSCOPY 1491-1500 (1985).

Commercial introduction by Schlumberger in 1987 of the "IDS 5000™" workstation-based, electron-beam test probe system greatly simplified E-beam probing of circuit chips and increased the efficiency of circuit debug. Among other features, the IDS 5000 system offers tools for "navigation" of an IC so that the e-beam can be rapidly and precisely placed to probe a location of interest while the IC is being electrically stimulated. See S.

CONCINA *et al.*, *Software Integration in a Workstation Based E-Beam Tester*, INTERNATIONAL TEST CONFERENCE PROCEEDINGS Paper 17.6 (1986); S. CONCINA *et al.*, *Workstation-Driven E-Beam Prober*, INTERNATIONAL TEST CONFERENCE PROCEEDINGS Paper 23.1 (1987); J. MCLEOD, *A New Tool Dramatically Cuts VLSI Debugging Time*, ELECTRONICS (April 30, 1987); N. RICHARDSON, *E-Beam Probing for VLSI Circuit Debug*, VLSI SYSTEMS DESIGN (August, 1987); S. Concina & N. Richardson *IDS 5000: an Integrated Diagnosis System for VLSI*, 7 MICROELECTRONIC ENGINEERING (1987); C. TALBOT, *VLSI Inspection Using Electron-Beam Imaging Systems*, PRODUKTRONIKA 87, SEN-SORIK (1987); and see U.S. Patents 4,706,019 and 4,721,909 to N. Richardson, which are incorporated herein by reference.

To summarize, an e-beam system such as the IDS 5000 system aids analysis of the operation of an IC, but does not offer the ability to modify the IC. Existing FIB systems offer the means to modify an IC, but pose difficulties in performing such steps as locating buried conductors, and determining when to terminate milling, and do not allow verification of the sufficiency of a repair.

SUMMARY OF THE INVENTION

It is an object of the present invention to overcome many of the limitations of the prior art as outlined above. It is further an object of the present invention to offer methods and apparatus useful in modifying electronic circuits such as ICs for failure analysis and the like. These and other objects are attained with embodiments of the methods and apparatus of the present invention.

In accordance with one form of the present invention, a system is provided which includes a chamber for receiving an IC, pump means for creating a vacuum in the chamber, means for applying a FIB to the IC, means for detecting charged particles (*e.g.*, secondary electrons or secondary positive ions) emitted as the FIB is applied to the IC, means for electrically stimulating the IC as the FIB is applied to the IC, and means responsive to the detector means for generating a voltage-contrast image of the IC and for linking the voltage-contrast image of the IC with a stored layout of the IC.

With such a system, it is possible to locate a conductor buried under dielectric material within the IC, by electrically stimulating the conductor and detecting secondary electrons emitted as the FIB is applied to the surface of the IC. It is also possible to use such a system for determining milling end-point when using the FIB, for example, to expose a buried conductor of the IC. The FIB is used to mill a hole (a "via") through overlying dielectric ma-

terial, and milling is terminated early, *e.g.*, before the buried conductor is expected to be exposed. The conductor is then electrically stimulated as the FIB is applied, and secondary electrons are detected to obtain a voltage contrast image. The voltage contrast image indicates whether the IC surface to which the FIB is applied is the conductor (DC voltage contrast exhibiting no capacitive decaying of the voltage contrast signal) or is the dielectric material (no signal or AC voltage contrast in which the voltage contrast signal decays over time). The steps are repeated until the voltage contrast signal indicates that the conductor is exposed, and are terminated before the conductor is severed. The technique improves the reliability of exposing a conductor without causing unintended damage.

It is further possible to use such a system to verify the repair of an IC step-by-step as the repair is made. When metal is deposited using the FIB for making electrical contact with a conductor of the IC, it is possible to verify that the contact is good by electrically stimulating the conductor as the FIB is applied to the deposited metal and emitted secondary electrons are detected. The resulting voltage contrast signal is indicative of whether the desired electrical contact has been achieved. The technique is useful in preparing pads for subsequent e-beam or mechanical probing, for example. Similarly, if two conductors are to be connected by depositing metal with the FIB, it is possible to first deposit metal in an effort to establish electrical contact with one of the conductors, then verify that the contact is good before depositing metal to complete the connection to the other conductor. Verification that intended connections are good enhances efficiency and the reliability of the IC modification process, and reduces the time needed to obtain functioning devices.

These and other features and advantages of the invention will become apparent to those of skill in the art from the following description of preferred embodiments of the invention and the accompanying drawing figures.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 is a functional block diagram of a preferred FIB system in accordance with the invention;

Figure 2 is a schematic diagram showing a preferred architecture of a FIB system in accordance with the invention;

Figure 3 is a more detailed functional block diagram of a FIB system in accordance with the invention;

Figure 4 is a partial, cross-sectional view showing principal elements of the FIB probe in accor-

dance with the invention;

Figure 5 is a schematic top view of the scintillator chamber of the FIB system in accordance with the invention;

Figure 6 is an exemplary user-interface display of the FIB system in accordance with the invention;

Figure 7 is a schematic diagram of a network including a focused ion beam system in accordance with the invention and an electron-beam test-probe system;

Figure 8A is a partial, sectional view of a portion of an IC being scanned by a FIB in SIM mode in accordance with a prior-art technique;

Figure 8B represents a SIM image of the IC portion of Figure 8A using the prior-art technique;

Figure 9A is a partial, sectional view of a portion of an IC being scanned by a FIB in SIM mode while being electrically stimulated, in accordance with the present invention;

Figure 9B represents a SIM image of the IC portion of Figure 9A in accordance with the present invention, showing the location of a buried conductor;

Figure 10 is a partial, sectional view of a portion of an IC, illustrating a structure to be modified;

Figure 11 is a partial, sectional view of a portion of an IC, illustrating a difficulty encountered in trying to expose a deeply buried conductor with a FIB in accordance with a prior-art technique;

Figure 12 is a partial, sectional view of a portion of an IC, illustrating a further difficulty encountered in trying to expose a buried conductor with a FIB in accordance with a prior-art technique;

Figures 13 and 14 are partial, sectional views of a portion of an IC, illustrating the results of inaccurate end-point detection when milling with a FIB to expose a buried conductor;

Figure 15 is a partial, sectional view of a portion of an IC, illustrating the result of correctly milling with a FIB to expose a buried conductor;

Figure 16 illustrates in a sequence of frames (a) through (g) a preferred technique for milling end-point detection in accordance with the present invention;

Figures 17, 18 and 19 illustrate exemplary signals obtained in carrying out the milling end-point determination technique illustrated in Figure 16; and

Figure 20 illustrates in a sequence of frames (a) through (h) a preferred technique for verification of IC repair with a FIB in accordance with the present invention.

The architecture of a preferred FIB system 110 is shown schematically in Figure 1. Such a system is preferably based on the architecture of an e-beam probe system such as an IDS 5000 system (available from Schlumberger Technologies of San Jose, California), to provide a convenient user interface and convenient access to the electronic circuit under test, but with a FIB probe substituted for the e-beam probe.

FIB system 110 has three main functional elements: a FIB probe 112, a circuit exerciser 114, and a data processing system 116 which includes a display terminal 118. An IC 126 is placed in a vacuum chamber 128 of FIB probe 112. Circuit exerciser 114 may be a conventional IC tester, such as a model "S-15™" tester available from Schlumberger Technologies, which can repeatedly apply a pattern of test vectors to IC 126 over a bus 124 in response to commands received from data processing system 116 over bus 110. The FIB can be aimed at a desired location on the IC in response to commands supplied from data processing system 116 over bus 122. A charged particle detector within the FIB probe 112 supplies measurements of secondary charged particles (e.g., secondary electrons or secondary positively-charged ions) energy to data processing system 116 over bus 122. Data processing system 116 may be used to specify the test signal pattern used and the timing of measurements relative to the test signal pattern. The electron-beam test probe system 110 is controlled by an operator who inputs commands through the display terminal 118.

As shown in Figure 2, the system may be made completely self contained, requiring only external electrical power and a vacuum chamber exhaust. Referring to Figure 2, FIB probe 112 comprises a FIB column 210, a charged-particle detector 214, a gas injection assembly (shown at 510 in Figure 5), and an electron-flood gun assembly (shown at 530 in Figure 5) mounted on a precision X-Y stage 216 for motion relative to an IC positioned in vacuum chamber 218. Vacuum chamber 218 receives the IC specimen, and is situated above evacuated scintillator chamber 220. The vacuum pumping subsystem, which consists of a rotary backing pump 222, a turbo pump 223 and an ion pump 212, is mounted internal to the system frame and is vibration-isolated from it. A suitable FIB column 210, commercially available from the FEI Company, Beaverton, Oregon, USA, is a conventional two electrostatic lens design and uses a gallium liquid metal ion source (LMIS) which operates at a current density of $\approx 1 \text{ A/cm}^2$.

FIB column 210 is controlled by data processing system 116 via column interface circuitry 224 and 226. Pumps 212, 222 and 223 are controlled by data processing system 116 via pump control-

DESCRIPTION OF THE PREFERRED EMBODIMENTS

lers 228. X-Y stage 216 is controlled by data processing system 116 via X-Y motor controllers 230 and encoder controllers 232. Data processing system 116 includes hardware interface circuitry 234 and an image processor 236.

For simplicity of illustration, connections between certain elements are not shown in Figure 2; the functional block diagram of Figure 3 illustrates principal elements and interconnections of the system. Data processing system 116 may comprise a Sun SPARC Station having an associated display terminal 118. Serial interface 234 and image processor 236 communicate via a VME bus 310 with a SPARC Station interface 315. SPARC Station interface 315 communicates with the SPARC Station via a SCSI bus 320. A serial link 325 provides communication between serial interface 234 and a gas subsystem controller 330, FIB column controller 335, high-voltage controller 340, vacuum controller 228, motor controller 230, and image/flood controller 345. A gas subsystem 350 is provided for selective introduction of gas into the specimen chamber, *e.g.*, a carbonyl gas which allows selective deposition of metal on an IC by application of the FIB. The image/flood controller 345 serves (a) to amplify the detected-electron signal from detector 214 and pass it to image processor 236 for processing into a voltage-contrast image, and (b) to control electron flood gun assembly 530 (Figure 5).

As shown in more detail in Figure 4, FIB column 210 is inverted and mounted on precision X-Y stage 216. X-Y stage 216 is driven by stepper motors under software control that provide 0.2 μm step resolution. This provides a direct link with navigation software that allows the user to rapidly and accurately locate internal nodes of a specimen IC directly from the computer-aided-design (CAD) layout and schematic database which is displayed on the screen of display terminal 118. Image pan commands are directly translated into X-Y stage movements to aim the FIB. A specimen IC 126 is electrically coupled to a load module 410 for receiving signals from tester 114.

Figure 5 is a cross-sectional view showing FIB column 210 and scintillator chamber 220. The gas injection assembly 510 of gas subsystem 350, charged-particle detector assembly 214, a gate valve actuator 520 and an electron flood gun 530 are all mounted on the scintillator chamber (see also Figure 3) below the floor of the specimen chamber 218. FIB column 210 is differentially pumped by ion pump 212. To speed pump-down of specimen vacuum chamber 218 after an IC is installed, a gate valve (see Figure 5) maintains FIB column 210 at high vacuum when vacuum chamber 218 is brought to atmospheric pressure 218.

The inverted moving column architecture and scintillator chamber configuration give good access

to the inside of the vacuum chamber thus allowing easy exchange between various specimen stages. The configuration also provides electrical access to the device in the vacuum chamber. The vacuum chamber is preferably of modular construction so that any of four specimen stages can be mounted, namely, a packaged part stage, a small specimen tilt stage and both manual and motorized precision wafer stages.

Image processor 236 digitizes a 10MHz video signal from detector assembly 214, calculates a real-time rolling average for image noise reduction, stores the result in one of four frame buffers and performs analog video multiplexing (chroma-key) with the SPARC workstation 100MHz color video to display the SIM (scanning ion microscope) image directly on the screen of workstation display terminal 118. Bit mapped software access is provided for each of the four frame buffers.

FIB system 110 is controlled in software from the display terminal 118. The user-interface is modeled on the IDS 5000 e-beam prober user-interface. FIB column adjustments such as alignment, focus, astigmatism and source saturation are readily automated in software. Figure 6 is a schematic representation of the display screen of terminal 118 showing key software tools:

- o FIB tool (bottom left) displays either a stored or live, 30 frames per second, black and white SIM image. Typically, device exposure time is minimized to reduce the undesirable effect of milling during imaging. The view of the device in the chamber that is displayed in FIB tool is interactively controlled by simple mouse-driven pan and zoom commands. Pop-up menus allow the user to control simple column functions including contrast, brightness, and focus. The user may also define interactively "cut and deposition" rectangles (*e.g.*, 610, 615 and 620).
- o Layout tool (bottom right) displays the CAD layout database created during the IC design process. Layout tool and FIB tool in normal operation are locked together. A simple image to database alignment procedure, usually between the four corners of the die and the layout database, corrects automatically for errors in die position, rotation and tilt caused by the IC package. Once alignment is complete, pan and zoom commands entered into either FIB tool or Layout tool are reflected in the other. The two images move in lock step with an error of $< 1 \mu\text{m}$. Layout tool also allows definition of "cut and paste" rectangles (*e.g.*, 625, 630 and 635) in the database coordinate reference frame rather than the non-ideal X-Y stage reference frame used in FIB tool.
- o Schematic tool (top right) displays the sche-

matic or netlist database. Schematic tool and layout tool are linked at the connectivity level. Thus nets highlighted in the one domain are automatically highlighted in the other tool.

- o Cross-section tool (top left) displays an idealized device cross-section that is graphically constructed from the layout database and knowledge of the layer ordering and thickness. The process specific information, that is, layer ordering and thickness etc. is available from Cadence' DRACULA technology description file (which is also used for the database preprocessing that is necessary to link the schematic and layout connectivity information). Cross-section tool is used as an aid to interpreting device cross-sections.

Each of the software tools uses the same basic mouse commands and provides access to system peripherals including both black and white, and color hardcopy (not shown).

Figure 7 shows a FIB system 110, an e-beam probing system 710 (such as an IDS 5000 system) and a data store 720 linked by a local area network 730, such as an Ethernet network. Connecting the FIB system in such a network allows easy exchange of data concerning an IC, so that an IC may be readily modified in FIB system 110 and further analyzed in e-beam probing system 710. As is presented in the previous sections, much of the present FIB system's software environment is identical to that used in e-beam probing. Linking both the FIB and e-beam probing systems with a network allows the user to directly take advantage of the compatibility between the two environments. That is both systems can be used in parallel providing maximum utilization while the advantages of software and hardware compatibility allow for rapid changeover of an IC between the systems.

In most applications the time spent on each system per IC is measured in hours. This is large compared to the typical system to system changeover time and vacuum chamber evacuation time, typically 10 to 15 minutes combined. Thus the time consumed in moving between compatible FIB and e-beam probing systems in most applications is more than compensated by the 2X improvement in overall systems utilization. The key factor in making the two separate systems approach a practical reality in the eyes of the user is a common user-interface. The networked approach also has the following advantages:

- o IC CAD databases used in navigation on both systems need only be preprocessed once, stored in one place (that is on either system or on a remote file server) and can be accessed readily by both systems over the network.
- o Cut and deposition rectangles can be defined

remotely from the FIB system on the e-beam probe where problems are first located and characterized.

- o The network additionally allows for exchange of, and common access to, digitized images, IC XY coordinates and failure analysis reports.

Device Stimulus During Repair

Figure 4 shows a device in the chamber of the FIB system that is being directly stimulated using, for example, a conventional VLSI tester and test head. This capability is important in FIB applications such as those described below.

Locating Buried Conductors

In semiconductor fabrication processes where the inter-layer dielectric material is used to planarize the IC's surface, conductors buried underneath the surface are often not visible in a conventional SIM image. To illustrate, Figure 8A is a partial, sectional view of a portion 810 of an IC which includes a conductor 820 "buried" within dielectric material 830, and a pair of conductors 840, 850 in a metallization layer located on the surface of dielectric material 830. A FIB 860 is scanned over the surface as charged particles (e.g., secondary electrons) 870 are detected by detector 880. Figure 8B represents a SIM image of IC portion 810 which would be obtained using conventional FIB techniques: conductors 840 and 850 are visible in the image due to greater secondary charged-particle emissions from their metal surfaces than from the surrounding dielectric material, but "buried" conductor 820 is not visible.

In accordance with the present invention, buried conductors are electrically stimulated with an AC signal (represented schematically by AC signal source 910) supplied to the IC from tester 114 so as to create voltage contrast, as illustrated in Figure 9A. AC signals on buried conductors are capacitively coupled to the surface of the IC and are readily visible in a voltage-contrast SIM image. Buried conductors can thus be easily and accurately located. Figure 9B represents a SIM image of IC portion which would be obtained in accordance with the present invention: conductors 840 and 850 are visible in the image, as is buried conductor 820. Because the AC voltage on conductor 820 is capacitively coupled to the surface, conductor 820 will appear in the SIM image during each cycle of the applied AC signal.

Locating a buried conductor in accordance with the invention may be summarized as follows: stimulating a buried conductor of an IC with an AC signal while scanning the surface of the IC with a

FIB and detecting secondary charged particles, and forming a voltage contrast image of the IC from the detected energy of the secondary charged particles, such that the buried conductor is identifiable from the voltage contrast image.

End-Point Detection

Figure 10 is a partial, sectional view of a portion 1010 of an integrated circuit, illustrating a structure to be modified. The structure is typical of a two-metal, single-poly CMOS process. As illustrated, the structure comprises polysilicon 1015 into which one or more semiconductor devices (not shown) may be diffused, covered by oxide 1020. A metal layer including conductors 1025 and 1030 lies above oxide 1020 and is covered by oxide 1035. A metal layer including conductors 1040 and 1045 lies above oxide 1035. Passivation 1050 covers oxide 1035 and conductors 1040 and 1045.

It may be desired, for example, to expose conductor 1045 by FIB milling of passivation 1050 (as shown by dashed lines at 1055) or to expose conductor 1030 by FIB milling of passivation 1050 and oxide 1035 (as shown by dashed lines at 1060).

Figure 11 illustrates a difficulty encountered in trying to expose a deeply "buried" conductor such as conductor 1030 with a prior-art technique. As the passivation 1050 and oxide 1035 are bombarded by ions from the FIB, material being milled away splatters out of the hole. However, as the hole becomes deeper, the amount of material which succeeds in leaving the hole declines and residue of the milled material begins to build up in the lower portion of the hole, as represented at 1110. Even if the somewhat higher secondary charged-particle emission from metal from conductor 1030 over that of oxide 1035 and passivation 1050 is detected by monitoring during milling, it is not certain that conductor 1030 will be adequately exposed to enable electrical contact.

Figure 12 illustrates a difficulty encountered in trying to expose any "buried" conductor such as conductor 1045 with a prior-art technique. If the FIB is not aligned perpendicular to the plane of the IC, it is possible to mill a hole at an angle, resulting in conductor 1045 being exposed, but at least partially milled away in the process.

Figures 13 and 14 illustrate still other difficulties encountered in trying to expose a "buried" conductor such as conductor 1045 with prior-art techniques. Conductor 1045 may remain insulated by a thin layer of material 1310 if the milling is terminated too soon (Figure 13), or may be completely severed if the milling continues too long (Figure 14). Either problem can inadvertently arise due to the imprecise nature of the FIB milling

process. Ideally, the milling should be just enough to expose the conductor without damaging it, as shown in Figure 15.

The voltage contrast phenomenon is also useful in performing end-point detection. Only AC voltage contrast is visible on buried conductors. DC voltage contrast is not visible on buried conductors but is visible on surface conductors, thus allowing buried and surface conductors to be readily differentiated. This fact allows determination of whether, for example, the dielectric material has been removed from a buried conductor and thus allows precise end-point detection of the milling process so that a buried conductor can be exposed in a more uniform and predictable manner.

Figure 16 illustrates in sequence (a) through (g) a preferred implementation. Frame 16(a) shows in section a portion of an IC in which a conductor 1610 is buried in a dielectric material 1615. A FIB 1620 is used to mill away dielectric material 1615 to form a hole 1625 as shown in Frame 16(b), but only to a "safe" depth which is sure to avoid milling conductor 1610. Conductor 1610 is then stimulated with an AC signal (represented schematically by AC source 1630) from tester 114, as secondary charged particles (e.g., electrons or positive ions) 1635 are detected by a detector 1640. The AC stimulus signal may comprise a test pattern for the IC which is cycled at a low frequency, e.g., 1 Hz. The voltage contrast signal from detector 1640 will be influenced by the applied AC signal due to capacitive coupling (represented schematically by capacitor 1645) through dielectric 1615 to the surface being milled; Figure 17 shows an example of a typical expected voltage contrast signal in which capacitive decay is evident.

The voltage-contrast signal is preferably displayed as a voltage-contrast image of the IC. The changing voltage on the stimulated conductor will cause the stimulated conductor to periodically change intensity in the voltage-contrast image. If the stimulated conductor is capacitively coupled to the surface of the IC, it will cause a "flash" of voltage contrast when changing state, e.g., its voltage contrast intensity will decay rapidly after each transition.

Milling continues as shown in Frame 16(d). Conductor 1610 is again stimulated with an AC signal (represented schematically by AC source 1630 in Frame 16(e)) from tester 114, as secondary charged particles 1635 are detected by detector 1640. The voltage contrast signal from detector 1640 will be influenced by the applied AC signal due to capacitive coupling (represented schematically by capacitor 1650) through dielectric 1615 to the surface being milled. Because the dielectric is now thinner the capacitance at 1650 is greater than that at 1645. Figure 18 shows an example of a

typical expected signal in which the voltage excursions are increased relative to those of Figure 17 but in which the decay due to capacitance 1650 remains evident.

The steps of frames 16(d) and 16(e) are repeated as many times as necessary, until the conductor is exposed by milling as shown in frame 16-(f). Conductor 1610 is again stimulated with an AC signal (represented schematically by AC source 1630 in frame 16(g)) from tester 114, as secondary charged particles 1635 are detected by detector 1640. The voltage contrast signal from detector 1640 will be directly influenced by the applied AC signal as conductor 1610 is exposed. Figure 19 shows an example of a typical expected voltage-contrast signal in which the AC signal applied to conductor 1610 is evident and in which no further capacitive coupling influence is present. When this stage is reached, the intensity of the stimulated conductor in the voltage-contrast image will no longer decay after each transition of the AC stimulus signal, e.g., the conductor's intensity will no longer "flash" in the voltage-contrast image.

The FIB current is preferably adjustable, so that it can be raised during milling (e.g., Frames 16(b), 16(d) and 16(f)) and reduced during signal detection (e.g., Frames 16(c), 16(e) and 16(g)). A typical beam-current range is from 100 pA to 4 nA. Increased current increases FIB spot size, making the milling faster and less precise. Decreased current decreases FIB spot size, making the miller slower but more precise.

Alternate embodiments are also possible, such as continuous electrical stimulation of the conductor and detection of secondary charged particles during milling, so that the end-point detection is continuous during the milling process. Also, it is possible to stimulate a buried conductor for locating it with the FIB, as described above, then continue to scan the FIB over the area to be milled so as to carry out the milling; secondary charged particles are continuously or periodically detected to form a voltage contrast signal (from which a voltage contrast image may be generated and displayed).

Repair Verification

The FIB IC repair success rate is well known to be poor (typically <50%) particularly when IC modifications are complex or extensive. Reliable end-point detection particularly on lower level conductor is frequently cited as the key issue. The ability to stimulate and electrically test a device during the FIB IC repair process improves the success rate by electrically verifying the repair step-by-step. If a particular step is found not to be functional, in many situations it can be corrected in

situ and the remainder of the repair procedure completed.

The present invention offers a technique for verifying IC repairs step-by-step as they are made. Figure 20 illustrates in frames (a) through (h) a preferred implementation. Frame 20(a) shows in section a portion 2010 of an IC in which conductors 2015 and 2020 are buried in a dielectric material 2025. For purposes of the example of Figure 20, it is desired to repair the IC by establishing electrical contact between conductors 2015 and 2020 using an FIB so that conductor 2015 will drive conductor 2020 when the repair is completed.

Accordingly, a FIB 2030 is directed to mill a hole 2035 to expose conductor 2020, as shown in Frames 20(b) and 20(c). The milling process is preferably carried out using the end-point detection technique described above, and therefore may involve additional steps not shown in Figure 20. A carbonylic gas is introduced into the vacuum chamber, and metal 2040 is selectively deposited in hole 2035 as shown in Frame 20(d). Before completing the electrical connection between conductors 2015 and 2020, conductor 2020 is driven with a signal (represented by a signal source 2045), while the FIB is operated in SIM mode (preferably at reduced beam current to avoid damage to the IC) with detector 2050 detecting emitted secondary charged particles (e.g., electrons or positive ions). Driving conductor 2020 may be accomplished, for example, by driving the IC with a test vector pattern from tester 114, the pattern being cycled at a low frequency such as 1 Hz. The voltage contrast signal from detector 2050 will indicate whether good electrical contact has been established between metal 2040 and conductor 2020: if DC voltage contrast is observed, the connection is good; if AC voltage contrast (e.g., from capacitive coupling) or no or weak voltage contrast is observed, the connection is bad. If the connection is bad, the effort to establish contact with conductor 2020 (e.g., the steps of Frames 20(a) through 20(e)) can be repeated until a good contact is verified.

Once a good contact is established between metal 2040 and conductor 2020, the repair process may continue. As shown for example in Frames 20-(f), 20(g) and 20(h), a hole 2055 is milled to expose conductor 2015 (preferably employing the end-point detection technique described above) and metal 2060 is deposited in an effort to establish contact between metal 2040 and conductor 2015. As conductor 2020 is to drive conductor 2015, a test vector pattern from tester 114 may again be applied to the IC and a determination made whether conductor 2015 is being driven by the signal on conductor 2020. Such determination may, for example, be made by again using the FIB in SIM

mode to monitor the signal on conductor 2020.

Variants of the repair verification process are possible. For example, it may be preferred to drill holes 2035 and 2055 (e.g., carry out the steps illustrated in Frames 20(b), 20(c), 20(f) and 20(g)) before depositing metal (Frame 20(d)), verifying connection (Frame 20(e)) and again depositing metal (Frame 20(h)). Also, it may be preferred to continuously or intermittently stimulate a conductor while metal is being deposited over it and while secondary charged particles are detected to produce a voltage-contrast signal; the voltage-contrast signal (or an image generated from it) can thus be monitored during the metal deposition process to determine whether the metal is deposited in electrical contact with the stimulated conductor.

Thus, in a variant of the example of Figure 20, it is possible to continuously or intermittently stimulate conductor 2020 and detect secondary charged particles while locating conductor 2020, while milling to expose conductor 2020 (Frames 20(b) and 20(c)), and while depositing metal over conductor 2020 (Frame 20(d)).

Conclusion

It can be seen that the present invention offers novel techniques for enhancing the efficiency and reliability of IC modification, particularly with respect to locating buried conductors, more reliably determining milling end-point, and verifying repairs step-by-step. While the additional steps of the present invention may in some cases increase the time needed to effect repair of an IC, the overall efficiency and yield of the repair process is expected to increase by avoiding failed repairs.

The foregoing description of preferred embodiments of the invention is intended to be illustrative only, and not as a limitation of the invention which is defined by the claims which follow. Those of skill in the art will recognize many modifications which may be made in the preferred embodiments within the spirit and scope of the claimed invention.

As used herein, an "electronic circuit" is intended to mean an integrated circuit, a hybrid circuit, an opto-electronic circuit, a multi-chip carrier module (MCM), or any other manufactured item having active and/or inactive elements and/or conductors which may be probed and/or modified with a FIB.

Claims

1. A focused-ion beam system, comprising:

- a. a chamber for receiving an electronic circuit,
- b. pump means for creating a vacuum in said chamber,

c. means for applying a focused-ion beam to an electronic circuit within said chamber,

d. detector means for detecting secondary charged particles emitted as said focused-ion beam is applied to an electronic circuit within said chamber,

e. circuit exerciser means for electrically stimulating an electronic circuit within said chamber as said focused-ion beam is applied to the electronic circuit within said chamber, and

f. means responsive to said detector means for generating a voltage-contrast image of an electronic circuit within said chamber, and for linking said voltage-contrast image with a stored layout of the electronic circuit.

2. The system of claim 1, further comprising means for displaying the linked voltage-contrast image and stored layout, for displaying cut and deposition markers in the displayed voltage-contrast image and displayed layout, and for controlling said focused-ion beam applying means to apply a focused ion beam to regions of the electronic circuit corresponding to the cut and deposit markers.

3. The systems of claim 2, further comprising means for introducing a carbonyl gas into said chamber as said focused-ion beam is applied to an electronic circuit within said chamber.

4. The system of claim 1, wherein said focused-ion beam applying means includes means responsive to control signals for aiming the focused-ion beam and means responsive to control signals for setting intensity of the focused-ion beam, further comprising control means for supplying aiming control signals to said aiming means and for supplying intensity control signals to said intensity-setting means.

5. The system of claim 4, wherein said pump means, said detector means and said circuit exerciser means are responsive to control signals from said control means, and wherein said control means further supplies control signals to said pump means for controlling vacuum in said chamber, to said detector means for controlling detection of secondary charged particles, and to said circuit exerciser means for controlling stimulation of an electronic circuit within said chamber.

6. The system of claim 4, wherein said control means is connected to receive a detection signal from said detector means, said control means including means for preparing a

voltage-contrast image of at least a portion of an electronic circuit within said chamber from said detection signal.

7. The system of claim 6, wherein said control means further includes means for displaying said voltage-contrast image and for storing and displaying images of corresponding portions of a layout and of a schematic diagram and of a process-layer cross-section of the electronic circuit. 5
8. The system of claim 6, further including an electron-beam probe system and a communication channel for exchanging data concerning an electronic circuit between said electron-beam probe system and said control means. 10
9. A method of locating a conductor buried under a dielectric material in an electronic circuit, comprising: 15
 - a. electrically stimulating the buried conductor;
 - b. scanning a focused-ion beam over the electronic circuit as the buried conductor is electrically stimulated; 20
 - c. detecting secondary charged particles emitted from the electronic circuit as the buried conductor is electrically stimulated and the focused-ion beam is scanned; and 25
 - d. generating from said detected secondary charged particles a voltage-contrast image to reveal the location of the buried conductor. 30
10. A method of milling with a focused-ion beam to expose a conductor buried under a dielectric material in an electronic circuit, comprising: 35
 - a. applying a focused-ion beam to the dielectric material overlying the conductor; 40
 - b. electrically stimulating the conductor;
 - c. detecting secondary charged particles emitted from the electronic circuit as the buried conductor is electrically stimulated and the focused-ion beam is applied; 45
 - e. generating from said detected secondary charged particles a voltage-contrast signal indicative of whether the conductor is exposed to the focused-ion beam. 50
11. The method of claim 10, wherein step b. comprises intermittently electrically stimulating the conductor.
12. The method of claim 10, wherein step b. comprises intermittently electrically stimulating the conductor by applying a test vector sequence to the electrical circuit. 55
13. The method of claim 10, further comprising: terminating application of the focused-ion beam when said voltage-contrast signal indicates that the conductor is exposed to the focused-ion beam.
14. A method of verifying connection between deposited metal and a conductor of an electronic circuit with a focused-ion beam, comprising the steps of:
 - a. depositing metal in the vicinity of a conductor of an electronic circuit by applying a focused-ion beam to the electronic circuit in the presence of a carbonyl gas;
 - b. electrically stimulating the conductor;
 - c. detecting secondary charged particles emitted from the electronic circuit as the conductor is electrically stimulated and the focused-ion beam is applied to the deposited metal; and
 - d. generating from said detected secondary charged particles a voltage-contrast signal, said voltage contrast signal having at least one characteristic indicative of whether the metal is electrically connected to the conductor.
15. The method of claim 14, wherein step b. comprises intermittently electrically stimulating the conductor.
16. The method of claim 14, wherein step b. comprises intermittently electrically stimulating the conductor by applying a test vector sequence to the electrical circuit.
17. A method of modifying an electronic circuit to establish electrical connection between a first conductor and a second conductor of an electronic circuit in which the first and second conductors are buried beneath a dielectric material, comprising the steps of:
 - a. applying a focused-ion beam to the dielectric material to expose a portion of said first conductor;
 - b. applying a focused-ion beam to the dielectric material to expose a portion of said second conductor;
 - c. depositing metal in the vicinity of the first conductor by applying a focused-ion beam to the electronic circuit in the presence of a carbonyl gas;
 - d. electrically stimulating the first conductor;
 - e. applying a focused-ion beam to the deposited metal as the first conductor is electrically stimulated;
 - f. detecting secondary charged particles emitted from the electronic circuit as the

first conductor is electrically stimulated and the focused-ion beam is applied to the deposited metal;

g. generating from said detected secondary charged particles a voltage-contrast signal, said voltage contrast signal having at least one characteristic indicative of whether the metal is electrically connected to the first conductor; and

h. depositing additional metal to establish electrical contact between the second conductor and the metal deposited in step c., by applying a focused-ion beam to the electronic circuit in the presence of a carbonyl gas.

18. The method of claim 17, further comprising the step of locating said first conductor prior to step a. by:

- i. electrically stimulating the first conductor;
- ii. scanning a focused-ion beam over the electronic circuit as the first conductor is electrically stimulated;
- iii. detecting secondary charged particles emitted from the electronic circuit as the first conductor is electrically stimulated and the focused-ion beam is scanned; and
- iv. generating from said detected secondary charged particles a voltage-contrast image to reveal the location of the first conductor.

19. The method of claim 18, wherein step a. comprises:

- i. applying a focused-ion beam to mill away a portion of the dielectric material overlying the first conductor;
- ii. electrically stimulating the first conductor;
- iii. scanning a focused-ion beam over the electronic circuit as the first conductor is electrically stimulated;
- iv. detecting secondary charged particles emitted from the electronic circuit as the first conductor is electrically stimulated and the focused-ion beam is scanned;
- v. generating from said detected secondary charged particles a voltage-contrast signal, said voltage contrast signal having at least one characteristic indicative of whether the first conductor is exposed to the focused-ion beam; and
- vi. repeating steps i. through v. until said voltage-contrast signal indicates that the first conductor is exposed to the focused-ion beam.

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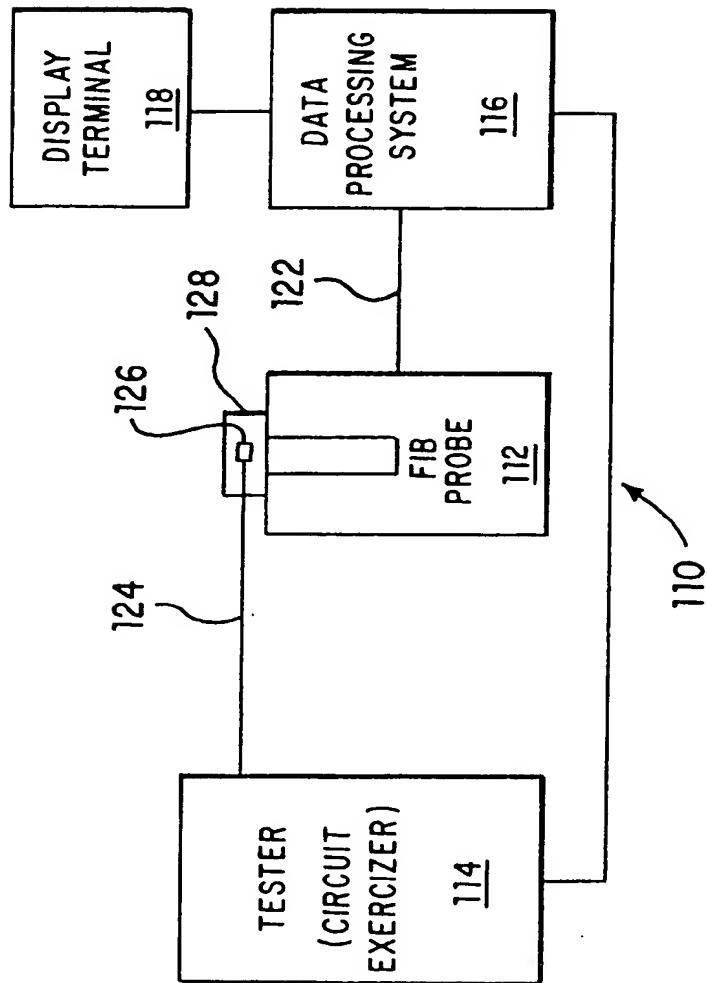


FIG. 1

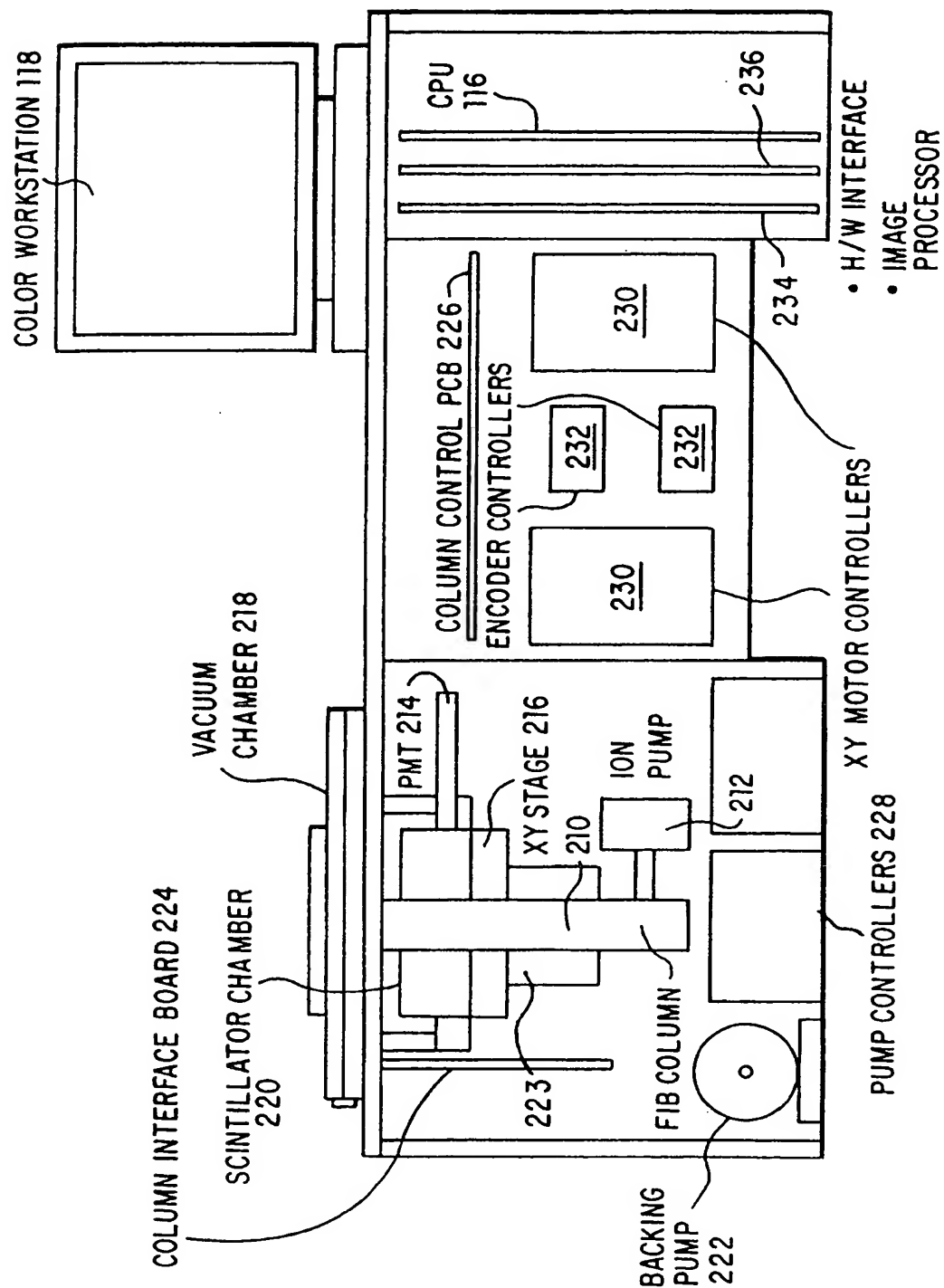


FIG. 2

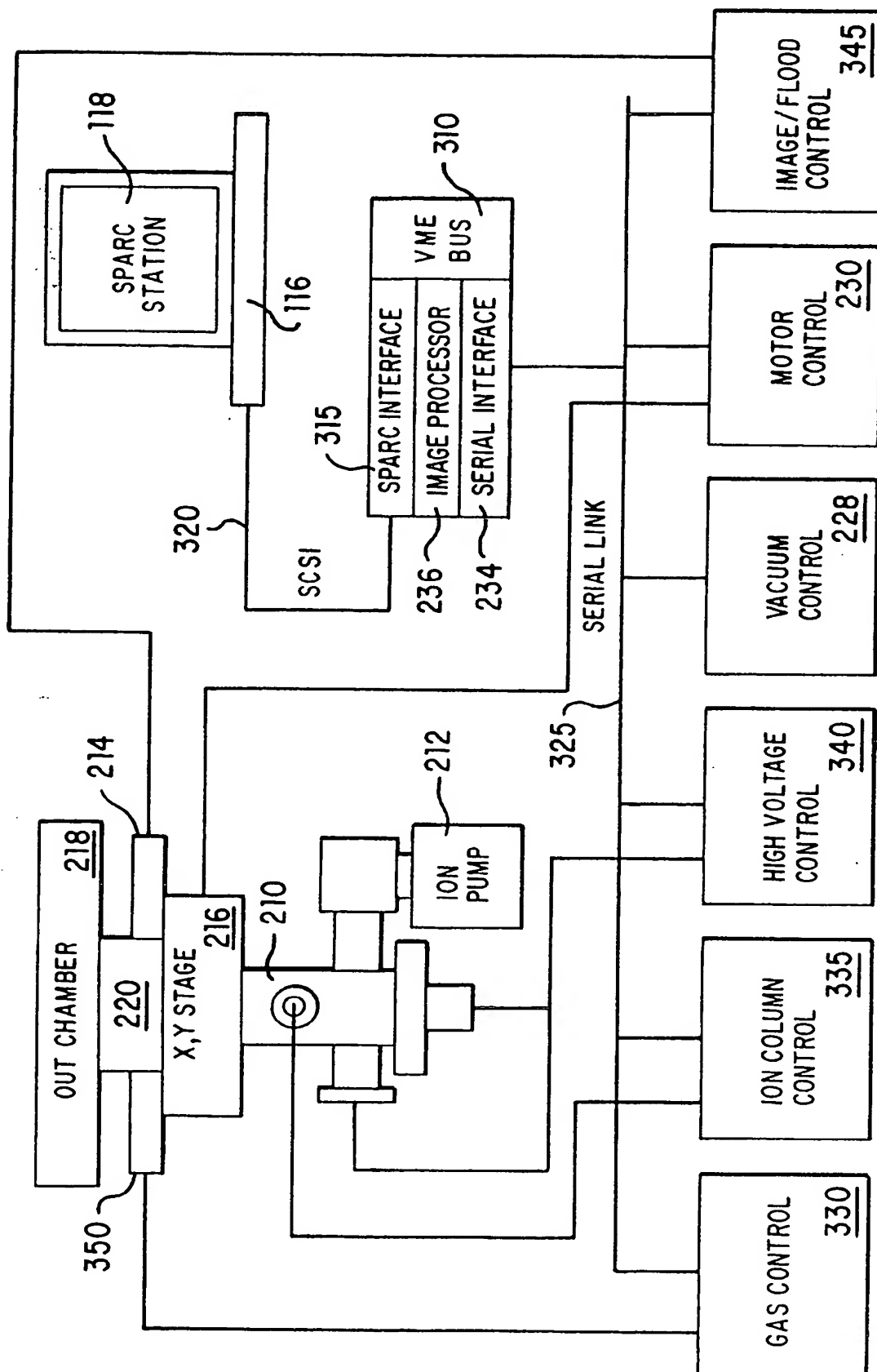


FIG. 3

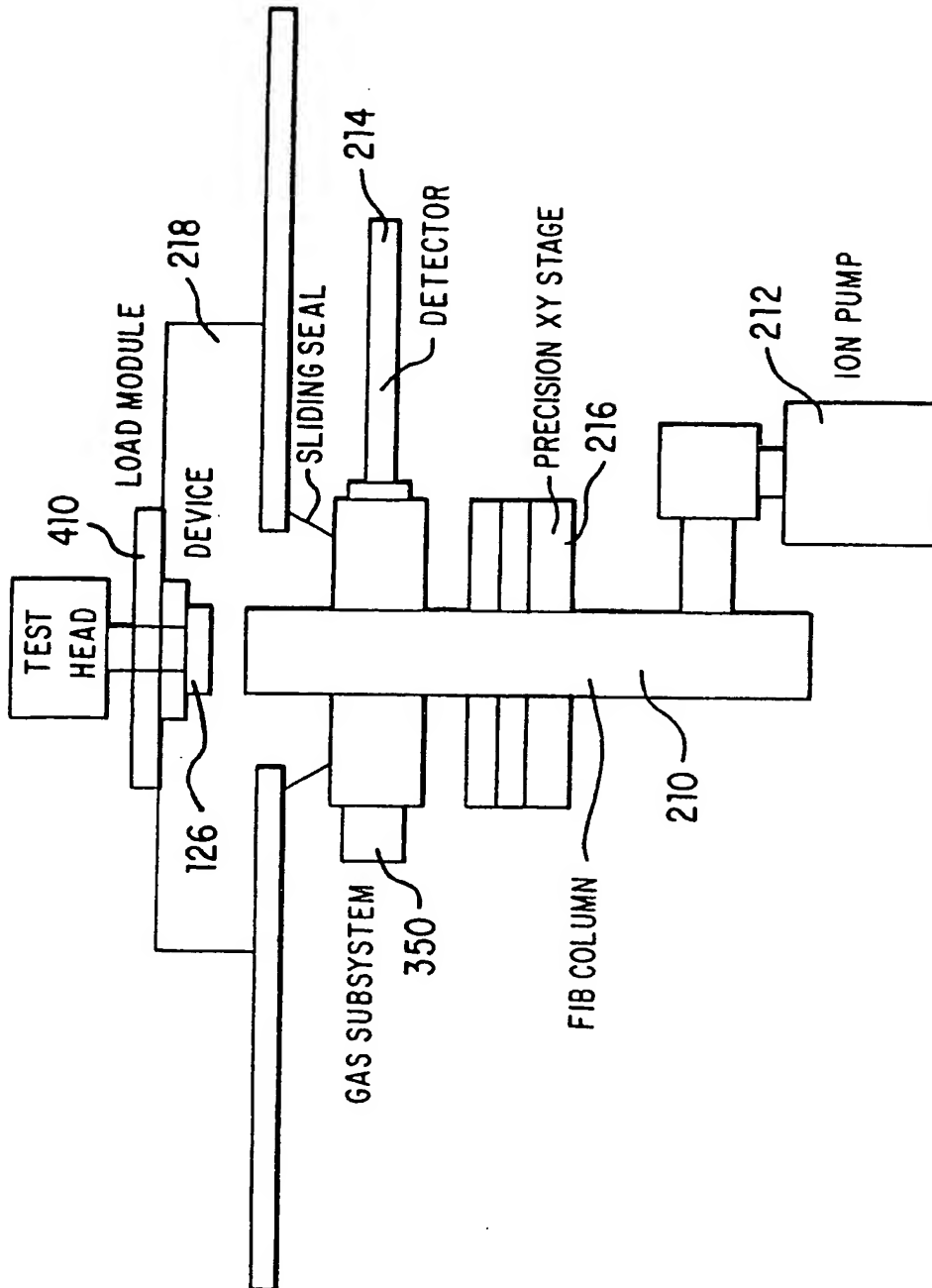


FIG. 4

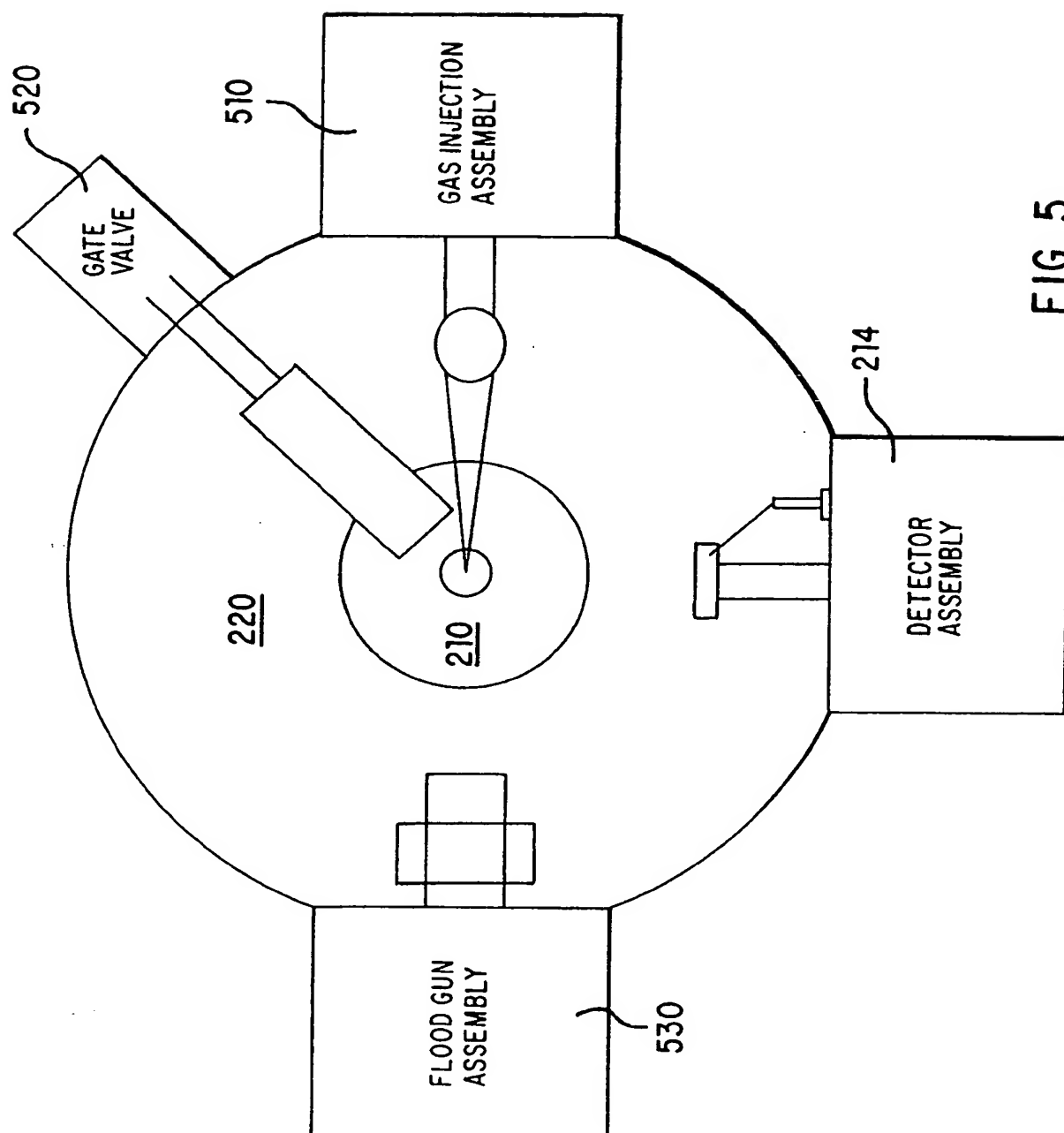


FIG. 5

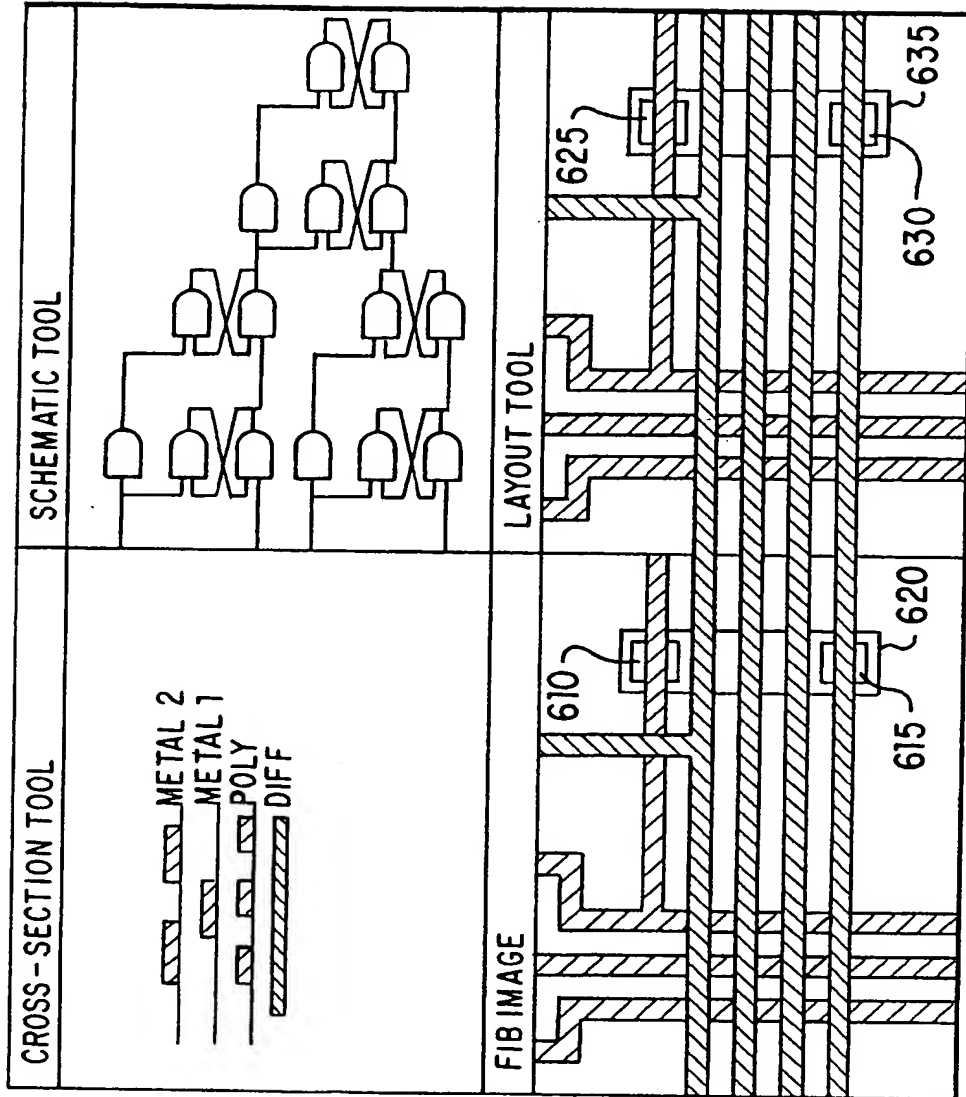


FIG. 6

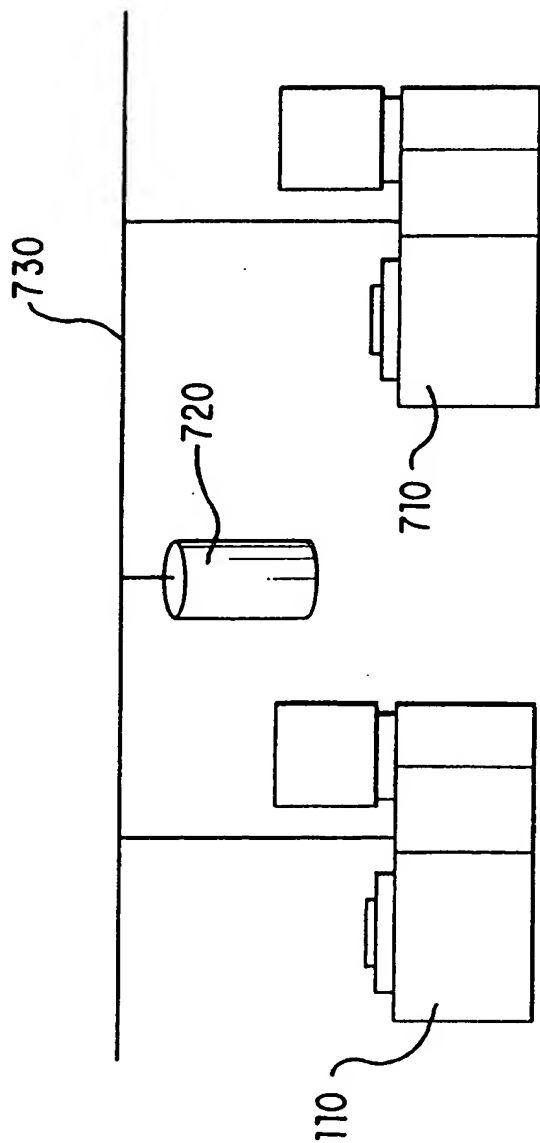


FIG. 7

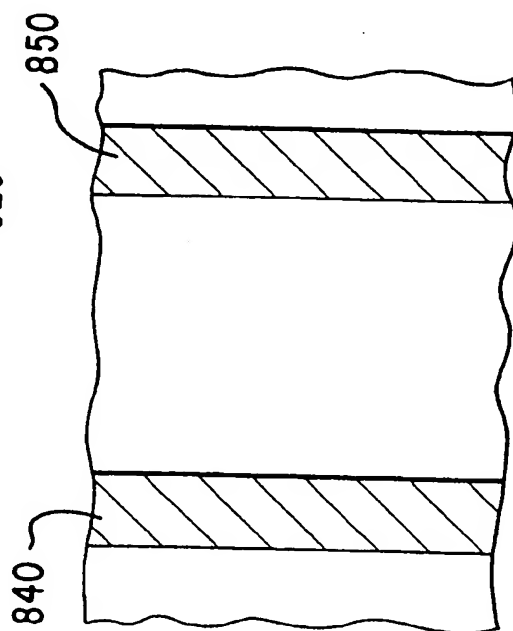
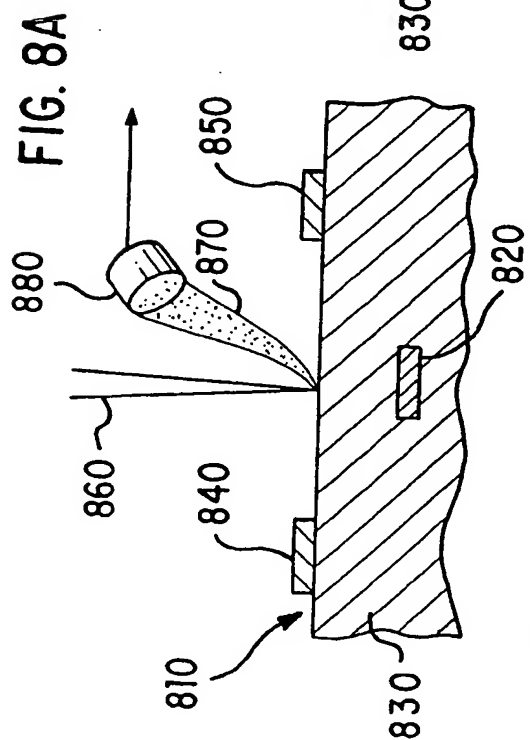
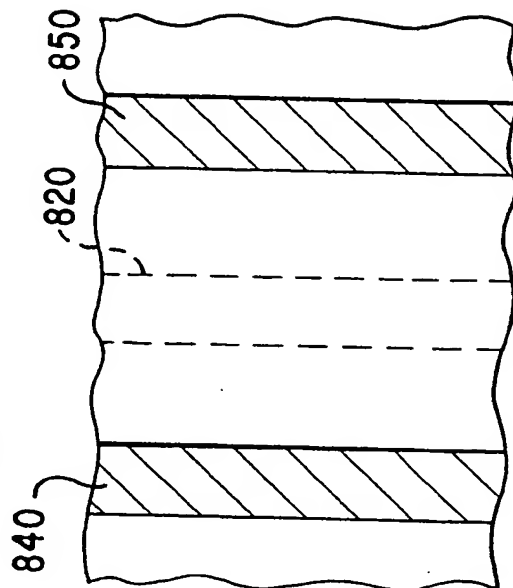
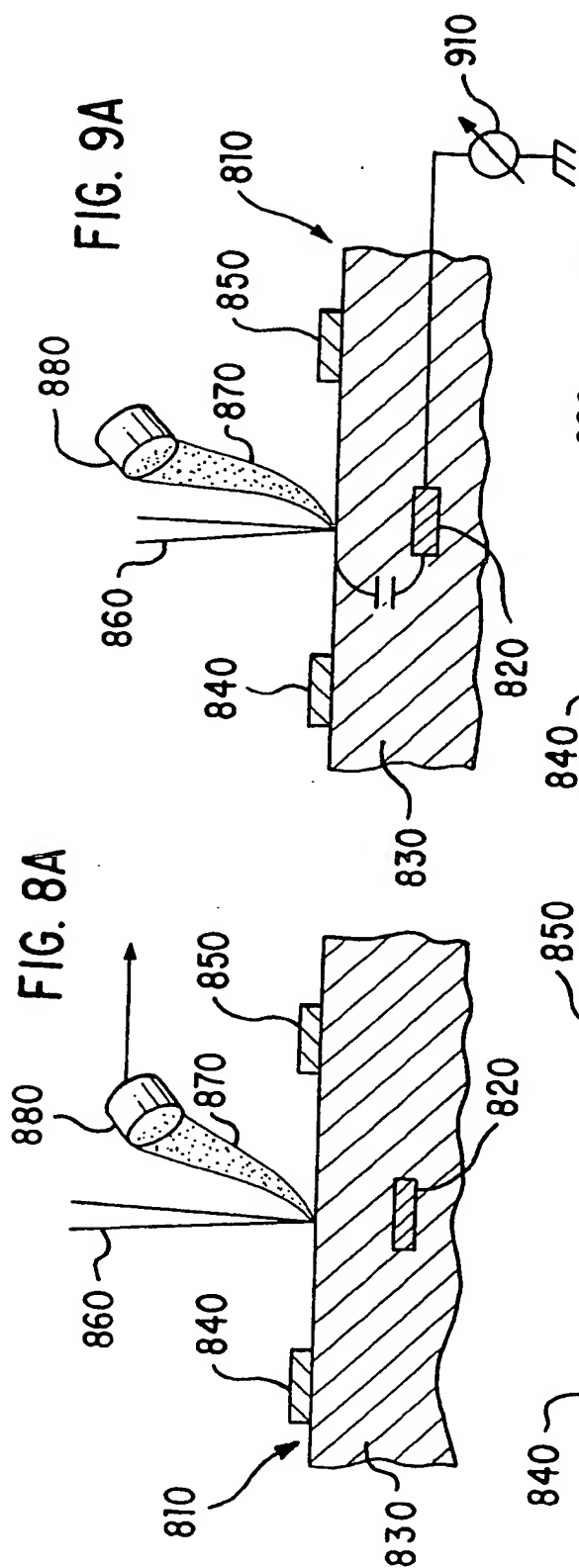


FIG. 13 PRIOR ART

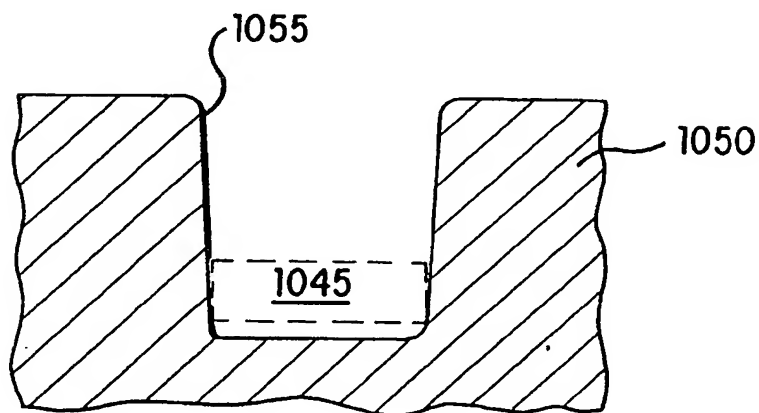
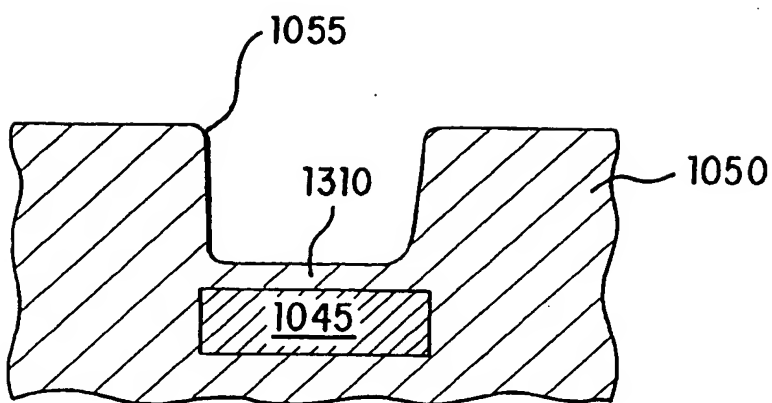


FIG. 14 PRIOR ART

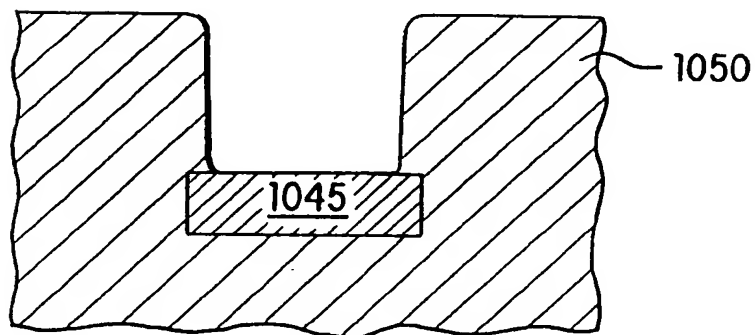


FIG. 15

FIG. 16(a)

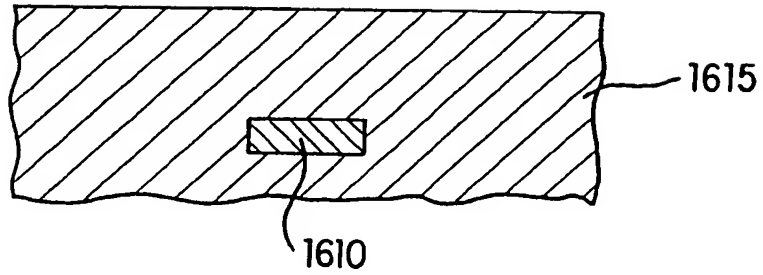


FIG. 16(b)

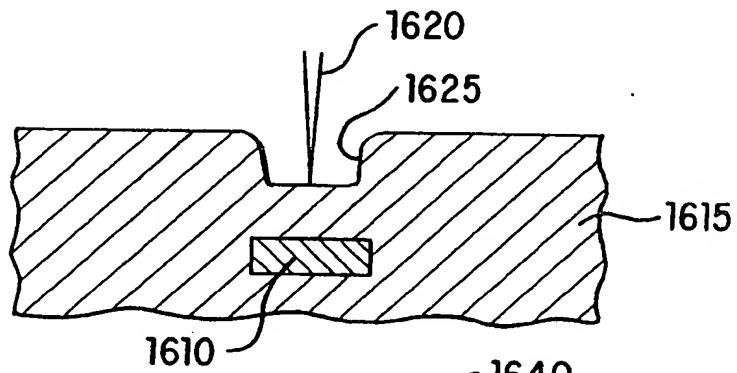


FIG. 16(c)

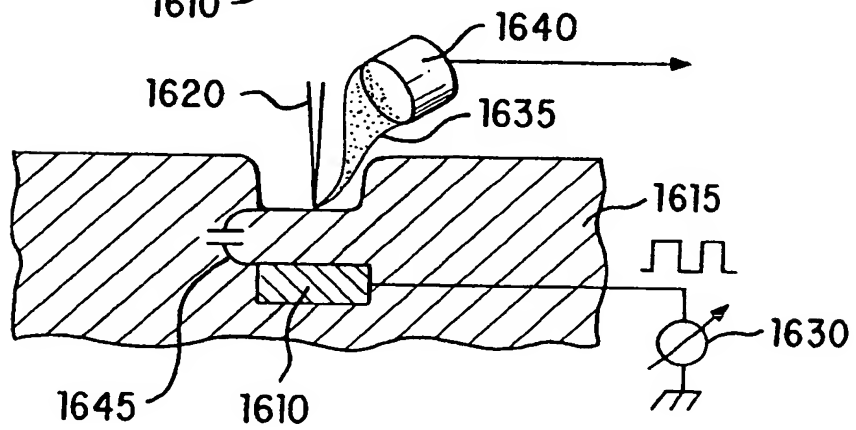


FIG. 16(d)

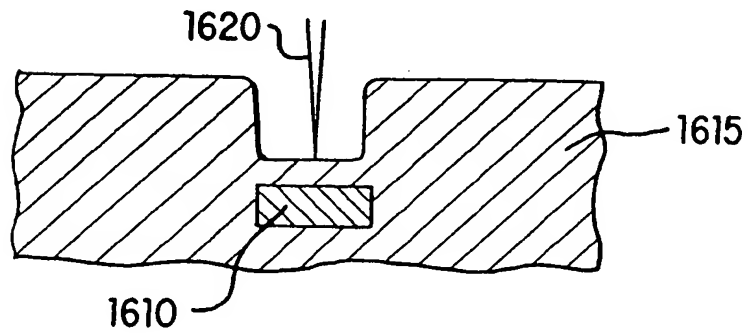


FIG. 16(e)

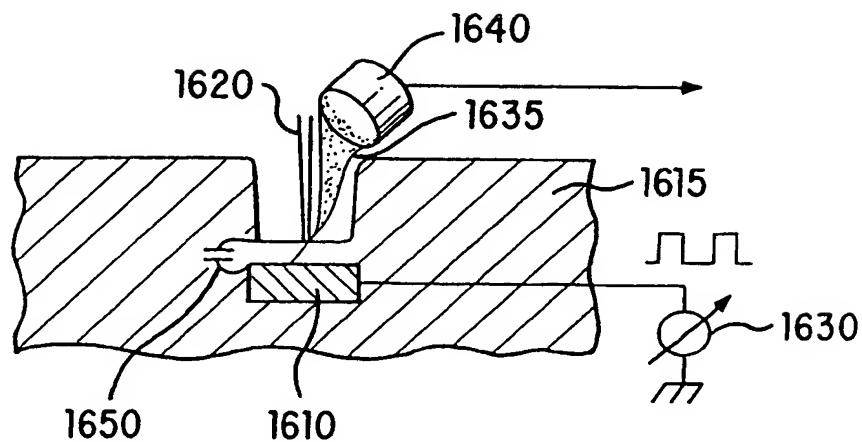


FIG. 16(f)

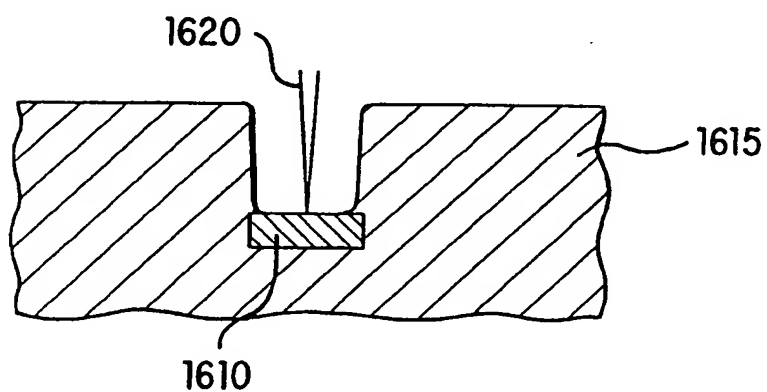


FIG. 16(g)

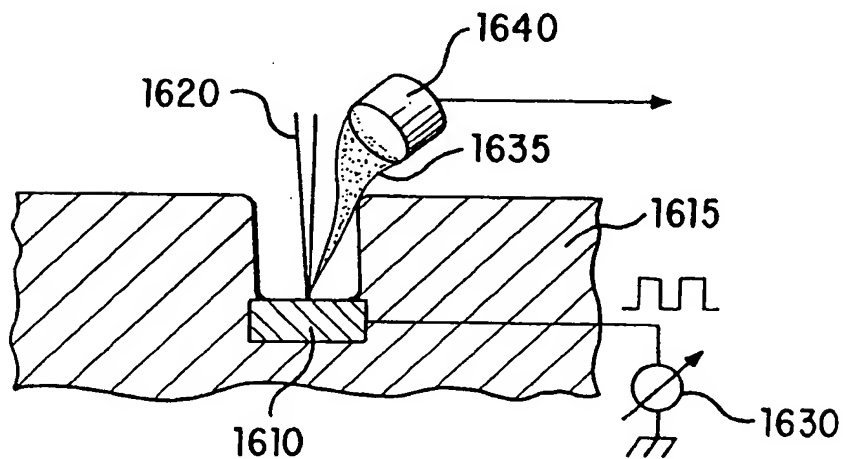


FIG. 17

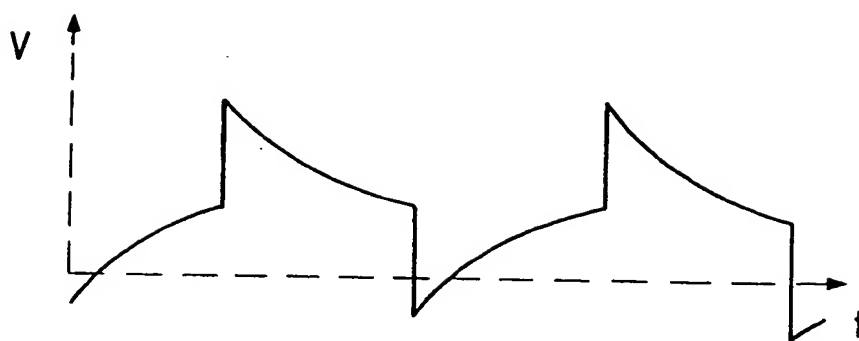


FIG. 18

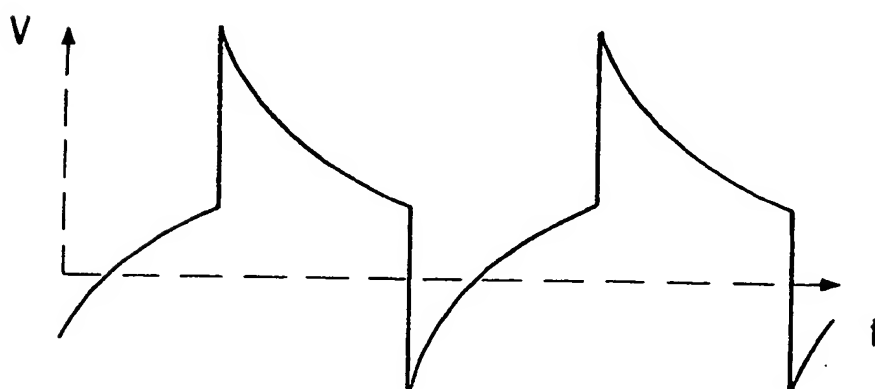
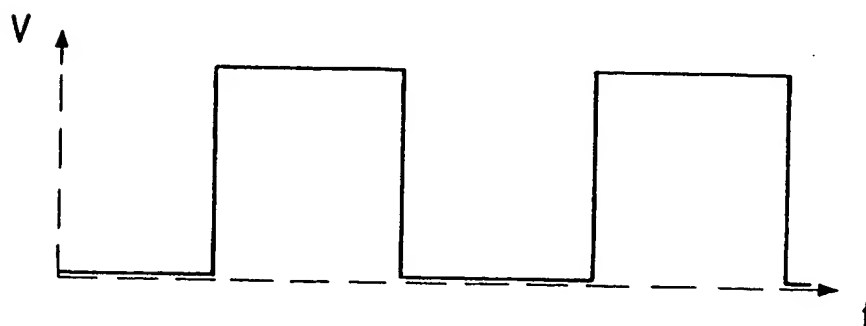
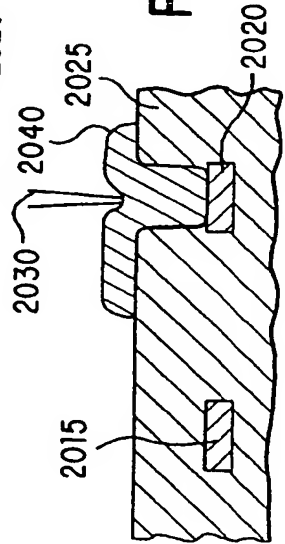
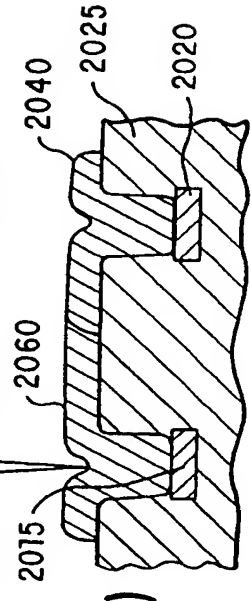
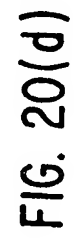
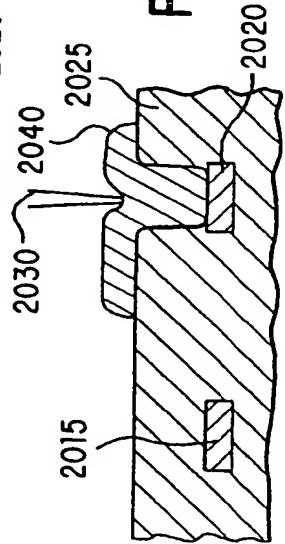
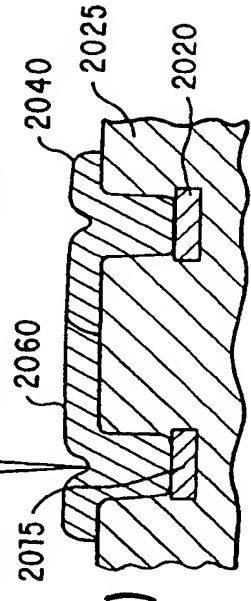
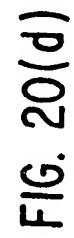


FIG. 19





(19)



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620-04
F-92542 Montrouge Cédex(FR)(54) **Integrated circuits modification with focused ion beam system.**

(57) Apparatus is provided which includes a FIB column having a vacuum chamber for receiving an IC, means for applying a FIB to the IC, means for detecting secondary charged particles emitted as the FIB is applied to the IC, and means for electrically stimulating the IC as the FIB is applied to the IC. The apparatus may be used, for example, (1) to locate a conductor (1610) buried under dielectric material (1615) within the IC, (2) for determining milling end-point when using the FIB (1620) to expose a buried conductor of the IC, and (3) to verify the repair of an IC step-by-step as the repair is made.

FIG. 16(a)

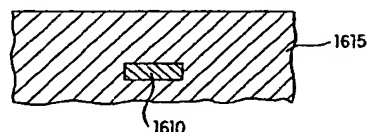


FIG. 16(b)

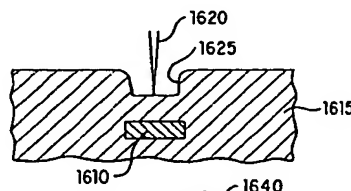


FIG. 16(c)

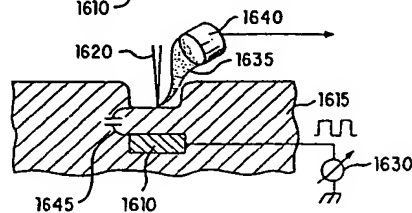
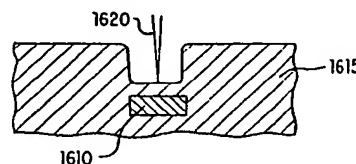
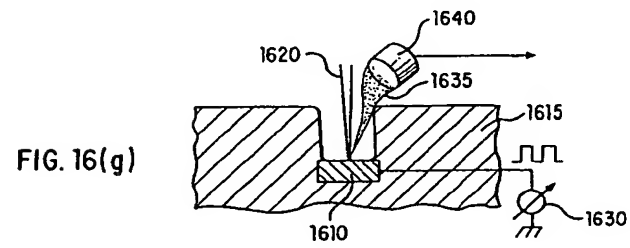
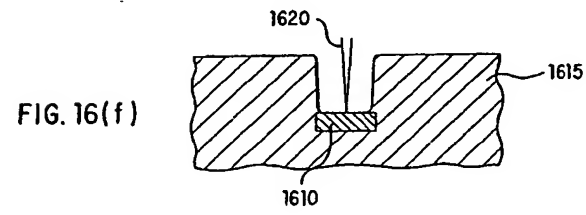
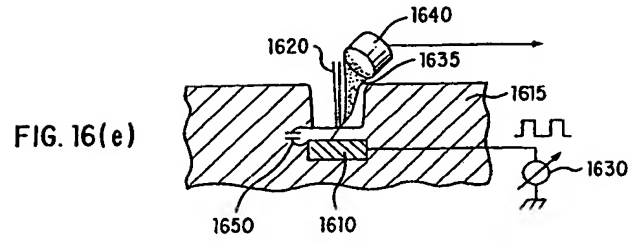


FIG. 16(d)



EP 0 495 262 A3





European Patent
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EUROPEAN SEARCH REPORT

Application Number

EP 91 20 3407

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	PATENT ABSTRACTS OF JAPAN vol. 8, no. 185 (E-262)24 August 1984 & JP-A-59 076 440 (FWITSU) 1 May 1984	1,9	H01J37/305 H01J37/30
A	 * abstract * ---	6,10,14, 17-19	
Y	EP-A-0 168 056 (HITACHI LTD.) * page 1, line 4 - page 2, line 19 * * page 4, line 10 - page 5, line 4; claims 1,2; figure 3 *	1,9 7,18	
P,A	US-A-5 055 696 (HARAICHI ET AL.) * abstract * * column 8, line 63 - column 9, line 35 * * column 10, line 22 - column 11, line 30; figures 6-10,38 * & JP-A-2 062 039 (HITACHI LTD.) ---	10,17	
A	WO-A-8 809 049 (MICROBEAM INC.) * abstract * * page 9, line 31 - page 10, line 1 * * page 12, line 33 - page 13, line 15; figure 4 *	3,17	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	WO-A-8 908 322 (MICRON CORP.) * page 1, paragraph 1 * * page 5, paragraph 3 * * page 17, line 24 - line 28; claims 13,14; figures 1,2 *	10,19	H01J
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 142 (E-254)3 July 1984 & JP-A-59 051 540 (HITACHI) 26 March 1984 * abstract * -----	14	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 06 JULY 1992	Examiner GREISER N.
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X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

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